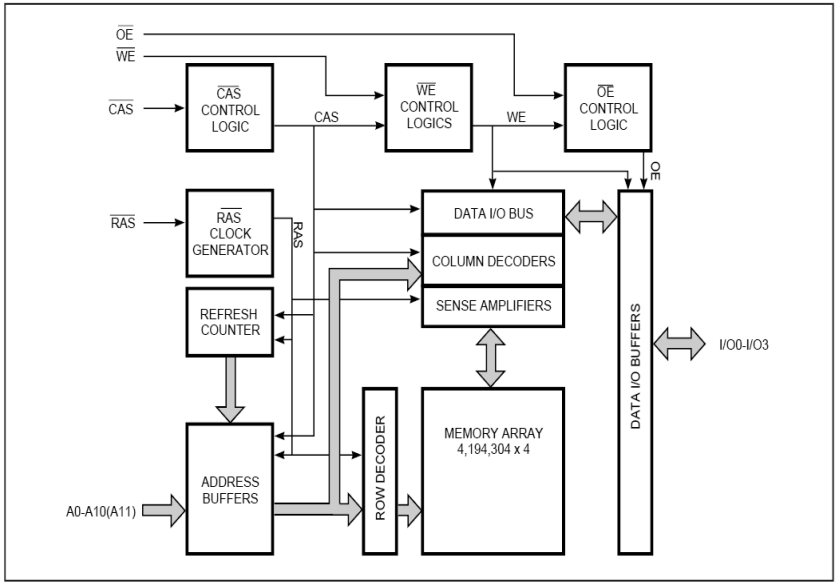
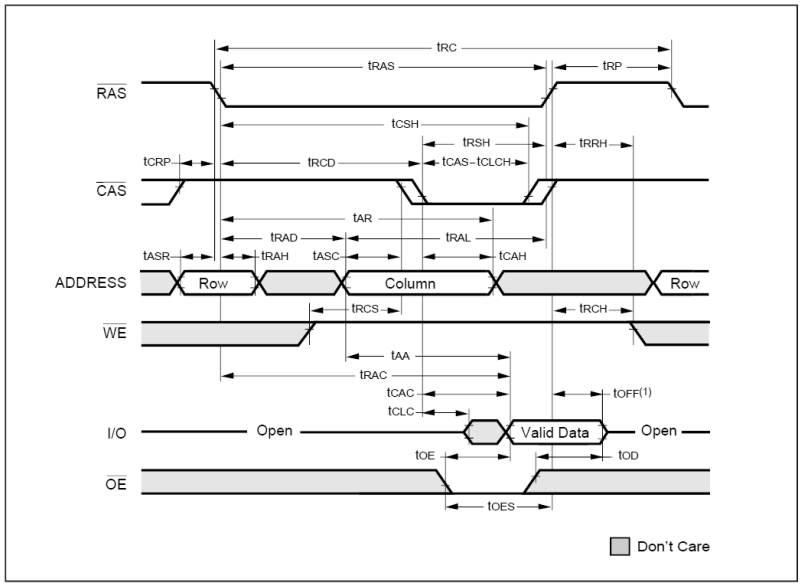
FUNCTIONAL BLOCK DIAGRAM



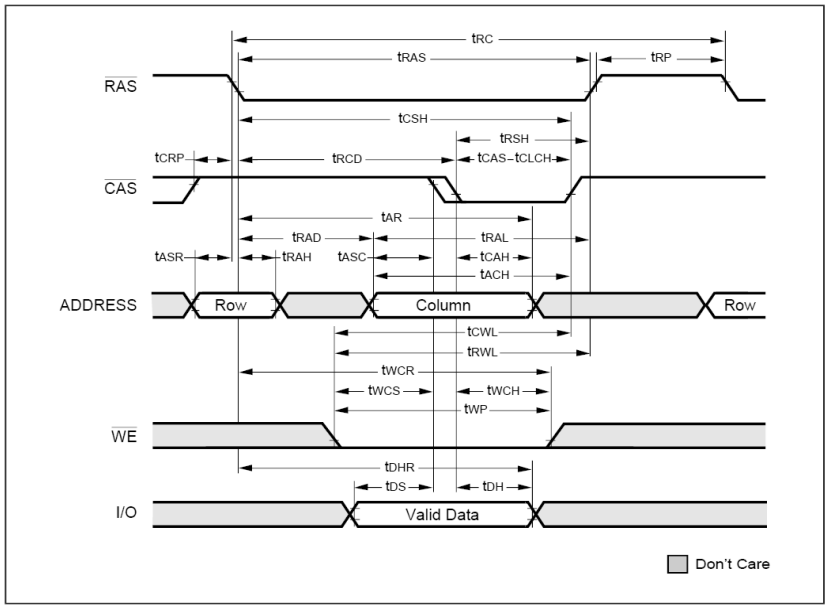
1

FAST-PAGE-MODE READ CYCLE



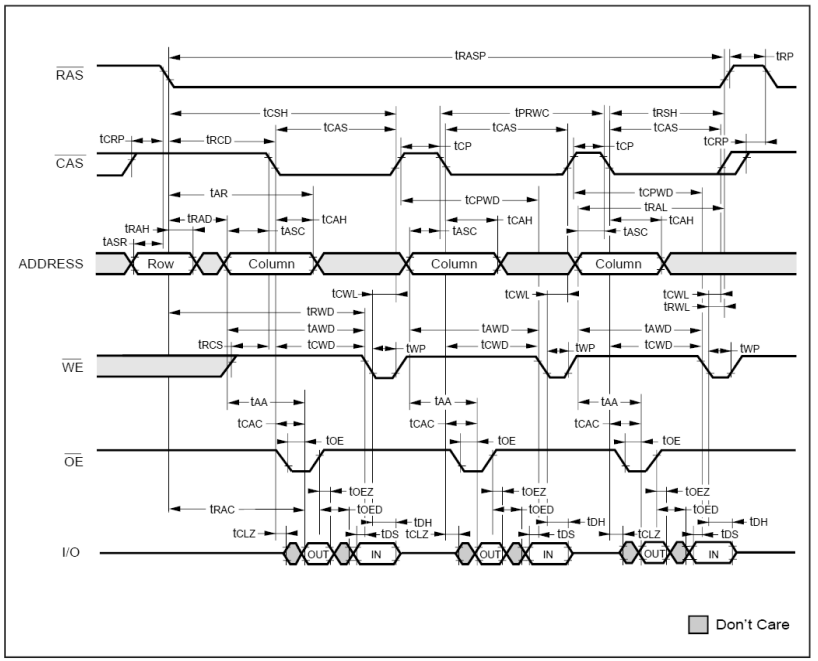
2

FAST-PAGE-MODE EARLY WRITE CYCLE (OE = DON'T CARE)



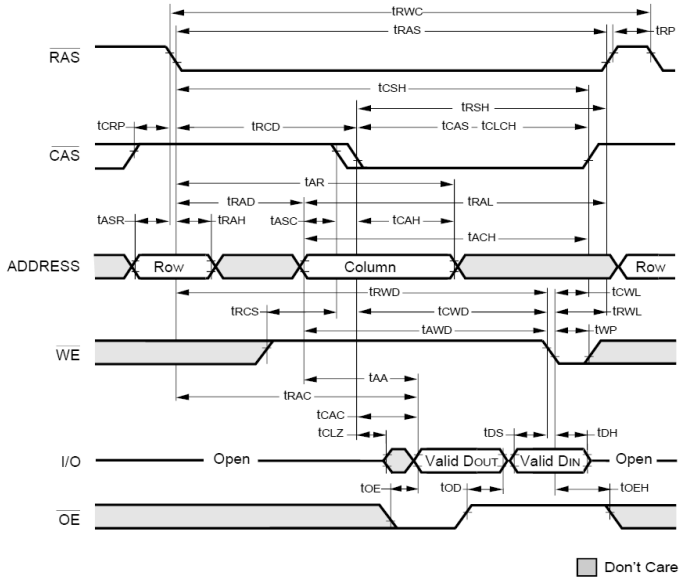
3

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

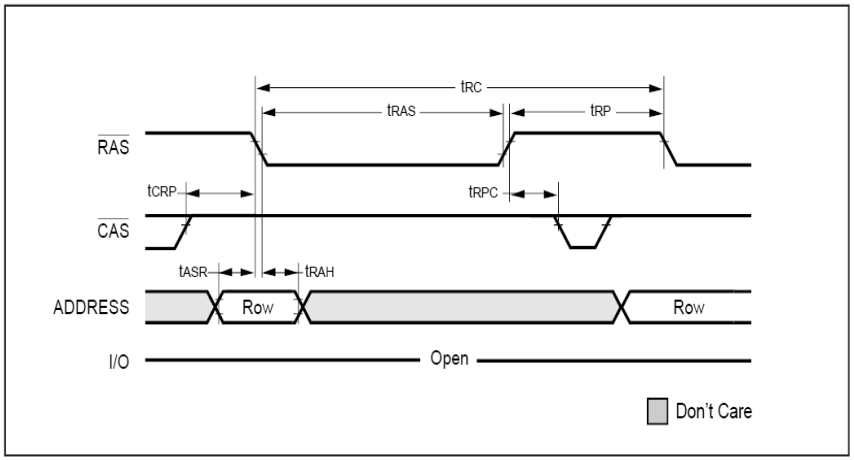


4

FAST-PAGE-MODE READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)



RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)



4M x 4 (16-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

FEATURES

- Fast Page Mode Access Cycle
- TTL compatible inputs and outputs
- Refresh Interval:
  -- 2,048 cycles/32 ms
  -- 4,096 cycles/64 ms
- Refresh Mode: RAS-Only, CAS-before-RAS (CBR), and Hidden
- JEDEC standard pinout
- Single power supply:
  5V ± 10% or 3.3V ± 10%
- Byte Write and Byte Read operation via two CAS

DESCRIPTION

The *ICSI* 4405x Series is a 4,194,304 x 4-bit high-performance CMOS Dynamic Random Access Memory. The Fast Page Mode allows 2,048 or 4096 random accesses within a single row with access cycle time as short as 20 ns per 4-bit word.

These features make the 4405x Series ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The 4405x Series is packaged in a 24-pin 300mil SOJ and a 24 pin TSOP-2

PRODUCT SERIES OVERVIEW

Part No.	Refresh	Voltage
IS41C44052	2K	5V ± 10%
IS41C44054	4K	5V ± 10%
IS41LV44052	2K	3.3V ± 10%
IS41LV44054	4K	3.3V ± 10%

KEY TIMING PARAMETERS

Parameter	-50	-60	Unit
RAS Access Time (tRAC)	50	60	ns
CAS Access Time (tCAC)	13	15	ns
Column Address Access Time (tAA)	25	30	ns
Fast Page Mode Cycle Time (tPC)	20	25	ns
Read/Write Cycle Time (tRC)	84	104	ns

IS41C16105
IS41LV16105

1M x 16 (16-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

FEATURES

- TTL compatible inputs and outputs; tristate I/O
- Refresh Interval: 1,024 cycles/16 ms
- Refresh Mode: RAS-Only, CAS-before-RAS (CBR), Hidden
- JEDEC standard pinout
- Single power supply:
  5V ± 10% (IS41C16105)
  3.3V ± 10% (IS41LV16105)
- Byte Write and Byte Read operation via two CAS
- Industrail temperature range -40°C to 85°C

DESCRIPTION

The *ICSI* IS41C16105 and IS41LV16105 are 1,048,576 x 16-bit high-performance CMOS Dynamic Random Access Memories. Fast Page Mode allows 1,024 random accesses within a single row with access cycle time as short as 20 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes the IS41C16105 ideal for use in 16-, 32-bit wide data bus systems.

These features make the IS41C16105 and IS41LV16105 ideally suited for high-bandwidth graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41C16105 and IS41LV16105 are packaged in a 42-pin 400mil SOJ and 400mil 44- (50-) pin TSOP-2.

KEY TIMING PARAMETERS

Parameter	-50	-60	Unit
Max. RAS Access Time (tRAC)	50	60	ns
Max. CAS Access Time (tCAC)	13	15	ns
Max. Column Address Access Time (tAA)	25	30	ns
Min. Fast Page Mode Cycle Time (tPC)	20	25	ns
Min. Read/Write Cycle Time (tRC)	84	104	ns