Figure 1: 128 Meg x 4 SDRAM Functional Block Diagram

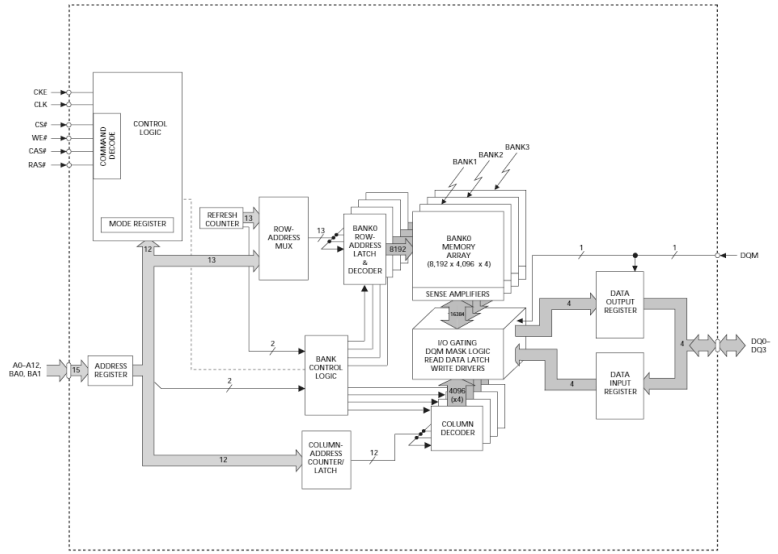


Figure 5: Mode Register Definition

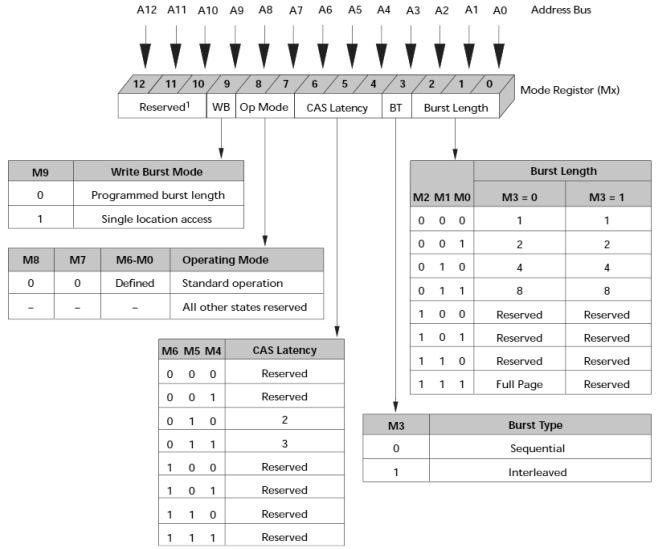


Figure 6: CAS Latency

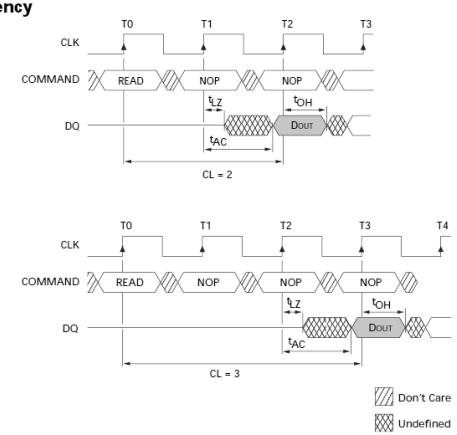


Table 5: CAS Latency

Speed	Allowable Operating Frequency (MHz)	
	CL = 2	CL = 3
-7E	≤ 133	≤ 143
-75	≤ 100	≤ 133

Table 6: Truth Table 1 – Commands and DQM Operation

Notes 1–2 apply to entire table; notes appear below

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	Address	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	4
Write enable/output enable	–	–	–	–	L	–	Active	8
Write inhibit/output High-Z	–	–	–	–	H	–	High-Z	8

Figure 7: Activating a Specific Row In a Specific Bank

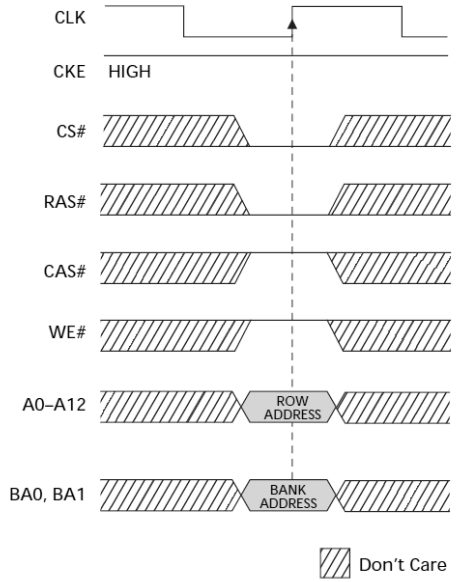


Figure 8: Example Meeting ^{t}RCD (MIN) when 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3

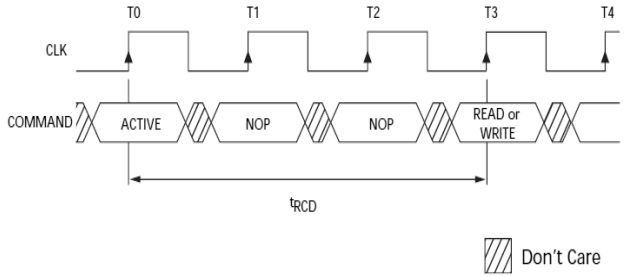
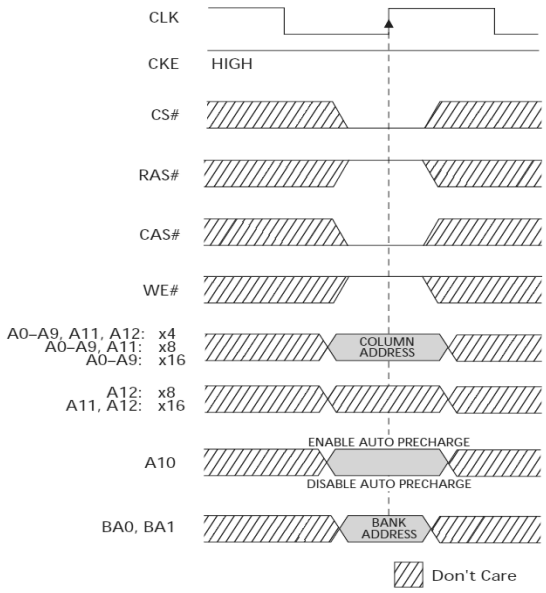
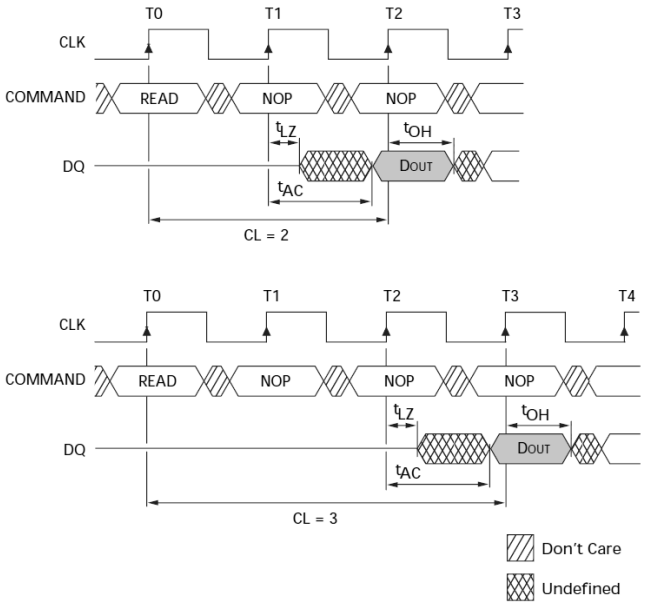


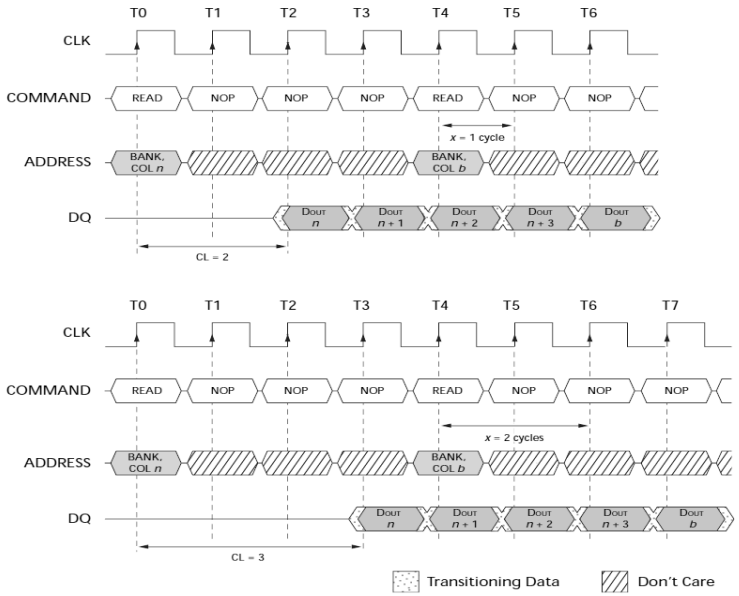
Figure 9: READ Command



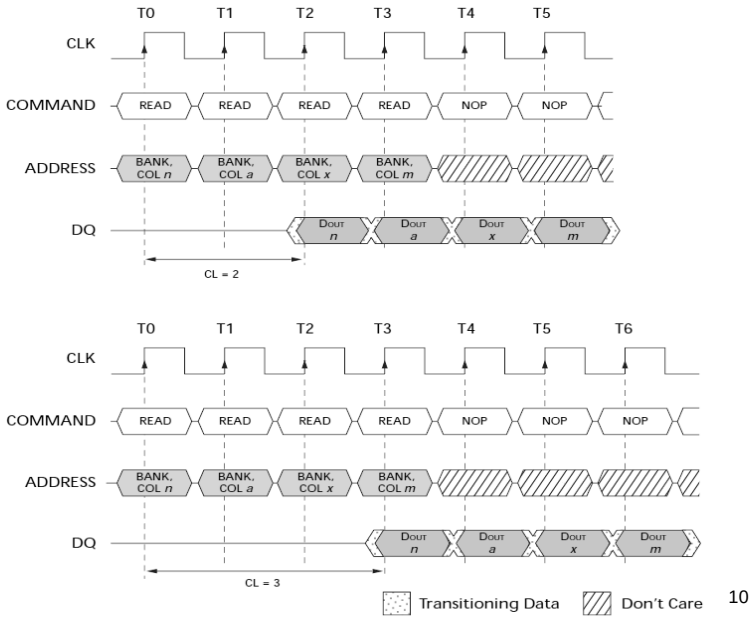
CAS Latency



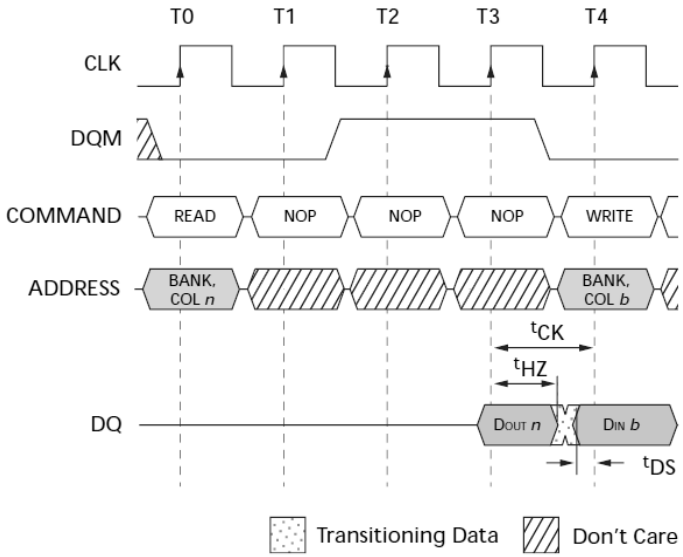
Consecutive READ Bursts



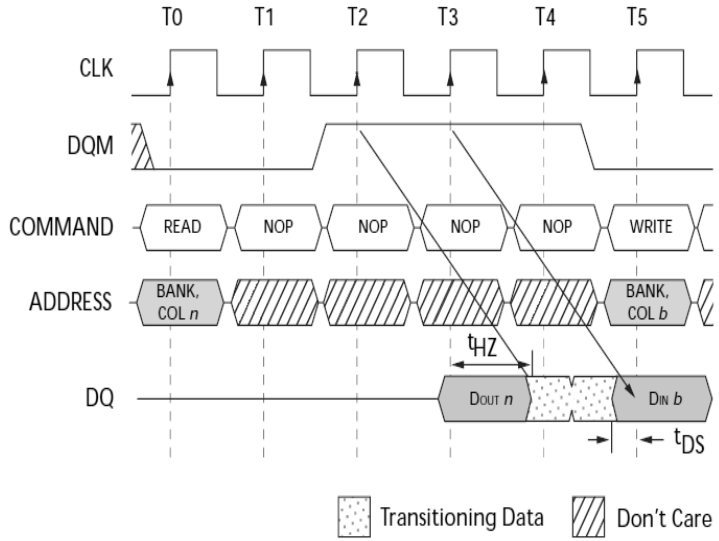
Random READ Accesses



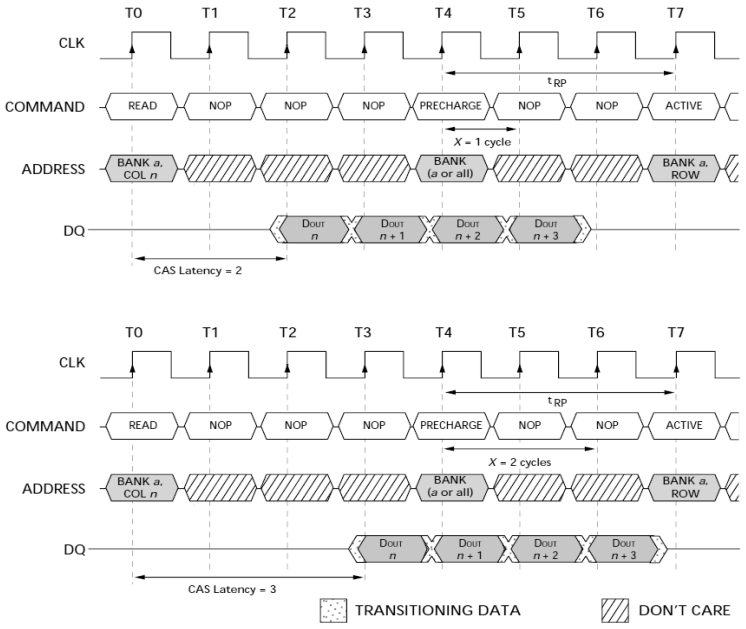
READ-to-WRITE



READ-to-WRITE with Extra Clock Cycle

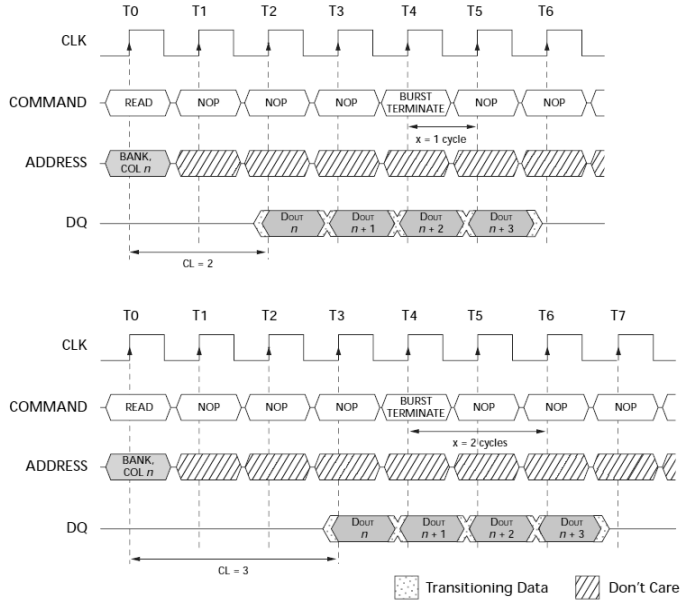


READ-to-PRECHARGE



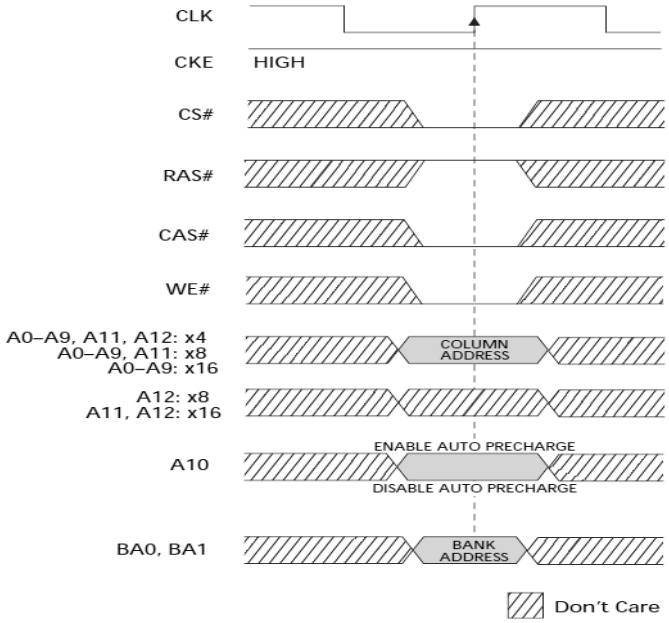
NOTE: DQM is LOW.

Figure 16: Terminating a READ Burst

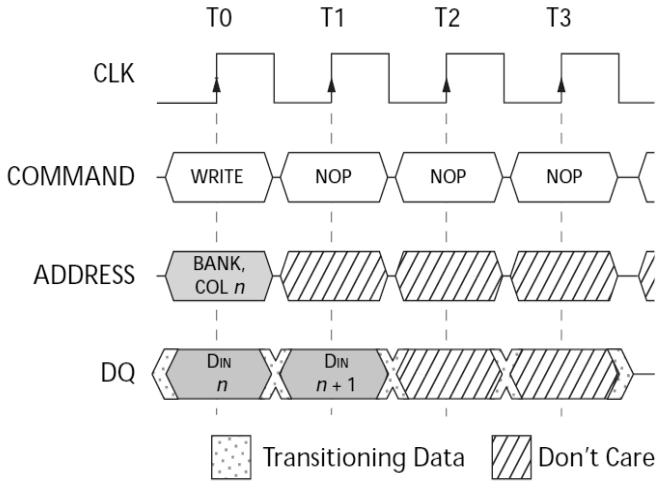


Note: DQM is LOW.

WRITE Command

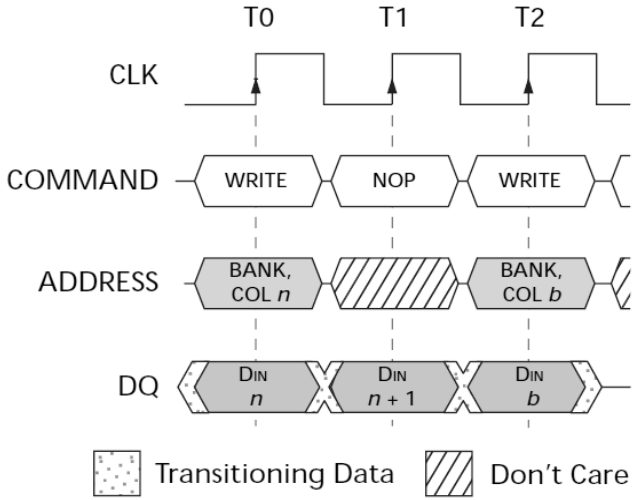


WRITE Burst

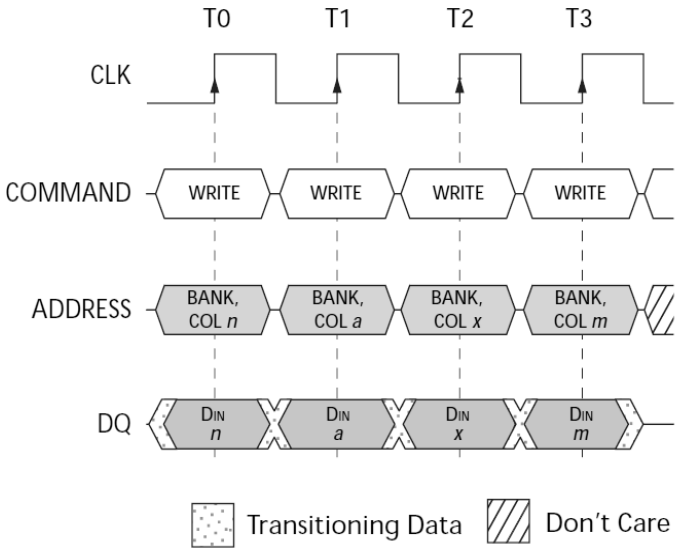


Note: BL = 2. DQM is LOW.

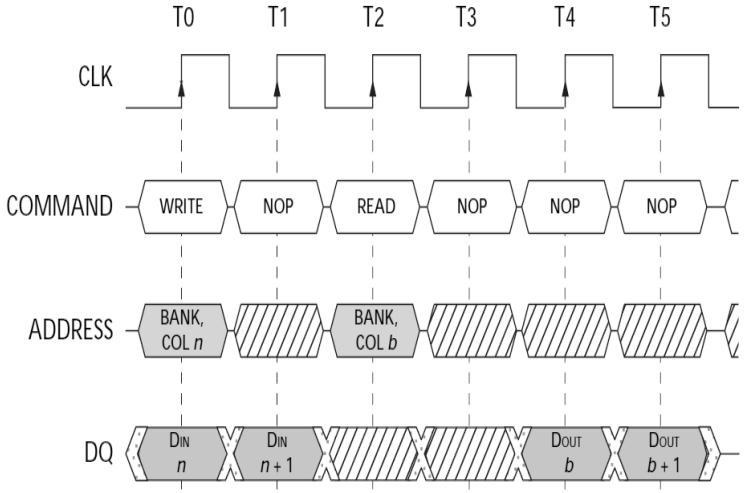
WRITE-to-WRITE



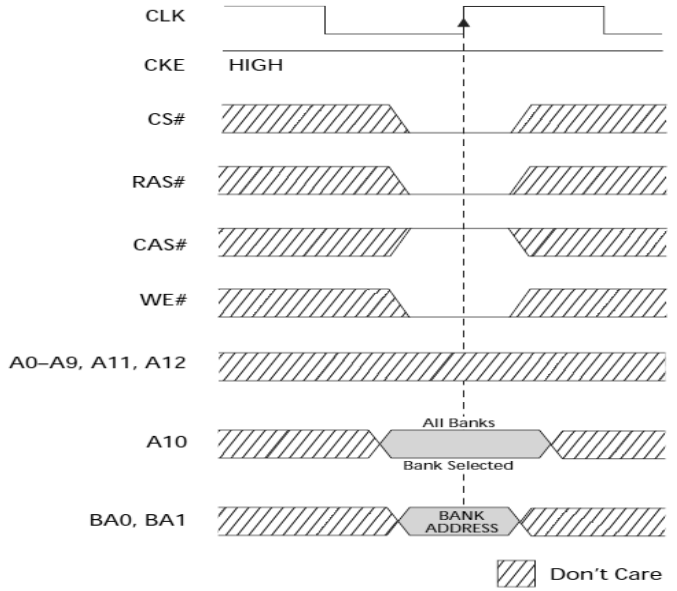
Random WRITE Cycles



WRITE-to-READ



PRECHARGE Command



Synchronous DRAM

MT48LC128M4A2 – 32 Meg x 4 x 4 banks
MT48LC64M8A2 – 16 Meg x 8 x 4 banks
MT48LC32M16A2 – 8 Meg x 16 x 4 banks

For the latest data sheet, refer to Micron's Web site

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode
- 64ms, 8,192-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

Options	Marking
• Configurations	
– 128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 32 Meg x 16 (8 Meg x 4 x 4 banks)	32M16
• WRITE recovery (^{t}WR)	
– ^{t}WR = "2 CLK"[1]	A2
• Plastic package – OCPL[2]	
– 54-pin TSOP II (400 mil)	TG
– 54-pin TSOP II (400 mil) Pb-free	P
• Timing (cycle time)	
– 7.5ns @ CL = 2 (PC133)	-7E[4]
– 7.5ns@ CL = 3 (PC133)	-75

Table 1: Address Table

Parameter	32 Meg x 4	32 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row addressing	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

Table 2: Key Timing Parameters

Speed Grade	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-7E	143 MHz	–	5.4ns	1.5ns	0.8ns
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	–	1.5ns	0.8ns
-75	100 MHz	6ns	–	1.5ns	0.8ns

Part Number Example:
MT48LC32M16A2P-75:C

- Self refresh
  - Standard — None
  - Low power — L[3]
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C +85°C) — IT
- Revision — :C

Notes: 1. Refer to Micron technical note: TN-48-05.
2. Off-center parting line.
3. Contact factory for availability.
4. Available on x4 and x8 only.

Table 3: Pin Descriptions

Pin Numbers	Symbols	Type	Description
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
18, 17, 16	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0–DQ7, and DQMH corresponds to DQ8–DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		

20, 21	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
23–26, 29–34, 22, 35, 36	A0–A12	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command (column-address A0–A9, A11, A12 [x4]; A0–A9, A11 [x8]; A0–A9 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether all banks are to be precharged (A10 [HIGH]) or bank selected by (A10 [LOW]). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0–DQ15	x16: I/O	Data input/output: Data bus for x16 (4, 7, 10, 13, 15, 42, 45, 48, and 51 are NCs for x8; 2, 4, 7, 8, 10, 13, 15, 42, 45, 47, 48, 51, and 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0–DQ7	x8: I/O	Data input/output: Data bus for x8 (2, 8, 47, and 53 are NCs for x4).
5, 11, 44, 50	DQ0–DQ3	x4: I/O	Data input/output: Data bus for x4.
40	NC	–	No connect: This pin should be left unconnected.
3, 9, 43, 49	$V_{DD}Q$	Supply	DQ power: Isolated DQ power to the die for improved noise immunity.
6, 12, 46, 52	$V_{SS}Q$	Supply	DQ ground: Isolated DQ ground to the die for improved noise immunity.
1, 14, 27	V_{DD}	Supply	Power supply: +3.3V ±0.3V.
28, 41, 54	V_{SS}	Supply	Ground.